IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Saul R. Dooley et al. Group Art Unit: 2611

Application No.: 10/564,422 Examiner: Dsouza, Joseph Francis A.

Filed: January 11, 2006 Confirmation No.: 8967

For: A METHOD OF CORRELATING A SAMPLED DIRECT SEQUENCE SPREAD SPECTRUM SIGNAL WITH A LOCALLY PROVIDED REPLICA

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REPLY BRIEF UNDER 37 C.F.R. § 41.41 (a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated April 28, 2009, which finally rejected claims 1-13 in the above-identified application. An Appeal Brief was filed on September 23, 2009. This Reply Brief is in response to the Examiner's Answer dated February 5, 2010. This Reply Brief is hereby submitted pursuant to 37 C.F.R. § 41.41(a).

CERTIFICATE OF MAILING UNDER 37 C.F.R. 1.8

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I. STATUS OF CLAIMS

No claims are canceled.

No claims are withdrawn.

No claims are objected to.

Claims 1-13 stand rejected as follows:

Claims 1, 2, 4, 6, 7, 9, and 11-13 stand rejected under 35 U.S.C. 102(b) as being anticipated by Medlock (U.S. Pub. Pat. No. 2001/0048713, hereinafter Medlock).

Claims 3 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock in view of Laudel et al. (U.S. Pat. No. 6,657,986, hereinafter Laudel).

Claims 5 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock in view of Harrison et al. (U.S. Pat. No. 5,982,811, hereinafter Harrison).

Claims 1-13 are the subject of this appeal. A copy of claims 1-13 is set forth in the Claims Appendix.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1, 2, 4, 6, 7, 9, and 11-13 are patentable over Medlock under 35 U.S.C. 102(b).

B. Whether claims 3 and 8 are patentable over the combination of Medlock and Laudel under 35 U.S.C. 103(a).

C. Whether claims 5 and 10 are patentable over the combination of Medlock and Harrison under 35 U.S.C. 103(a).

III. ARGUMENT

For the purposes of this appeal, claims 1, 2, 4, 6, 7, 9, and 11-13 are argued together as a group for purposes of the question of patentability over Medlock under 35 U.S.C. 102(b). Claims 3 and 8 are argued together as a separate group for purposes of the question of patentability over the combination of Medlock and Laudel under 35 U.S.C. 103(a). Claims 5 and 10 are argued together as a separate group for purposes of

the question of patentability over the combination of Medlock and Harrison 35 U.S.C. 103(a).

A. Claims 1, 2, 4, 6, 7, 9, and 11-13 are patentable over Medlock because Medlock does not disclose all of the limitations of the claims.

Appellants respectfully assert that claim 1 is patentable over Medlock because Medlock does not disclose all of the limitations of the claim. Claim 1 recites:

> A method of correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code, the method comprising:
>
> combining the bit or bits of at least two signal samples of the received signal to form a first word;
>
> providing a second word containing bits corresponding to the replica signal; and
>
> executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value.
>
> (Emphasis added.)

In contrast to the language of the claim, Medlock does not disclose all of the limitations of the claim because Medlock does not disclose carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value. Nevertheless, the Examiner persists in the assertion that Medlock purportedly performs word-based operations based on the description in Medlock of performing parallel operations. However, there appears to be a fundamental mischaracterization of the description of Medlock by the Examiner that underlies the Examiner's reliance on the description of performing parallel operations. This mischaracterization is evident in the following assertion:

> Regarding claim 1, Medlock discloses…
> Combining the bit or bits of at least two signal samples of the received signal to form a first word ([0029], Fig. 2A, element 203a; wherein the combination of bits of the samples is the bit slices);
>
> Advisory Action, 2/5/10, page 3 (original emphasis removed, underlining added.)

For contextual reference, the cited portion of Medlock generally relates to a fast searcher to parallely search for a phase offset between a first and second signal. Medlock, paragraph 27, lines 4-6. One of the signals is code sequence of a received input signal 208, and the other signal is an internally generated code sequence 210. Medlock, paragraph 28, lines 12-17. Fig. 2A illustrates the received input signal 208 (i.e., input data 208) and the internally generated code sequence 210 (i.e., code sequence 210) received by the fast searcher 120a.

Within the fast searcher, there are multiple computing circuits 204-1 through 204-N. Medlock, Fig. 2. Each computing circuit 204 performs bit-wise operations on one bit from the input data 208 and one bit from the code sequence 210. This is the meaning of the explicit statement that the multiply-logic devices perform operations on a chip-by-chip basis, as explained in Appellants' Appeal Brief. Medlock, paragraph 42, lines 12-14.

It should also be noted that the operations performed by the various computing circuits 204, even if operated in parallel, do not function to combine bits to form a word. Rather, each computing circuit 204 merely performs an operation on a single bit from the input data 208 and a corresponding bit from the code sequence 210. The process of sending the same bit of the input data 208 to the different computing circuits 204 does not disclose combining bits from the input signal 208 to form a word because there is no description of combining different bits of the input signal 208 at any point within the computing circuits 204 or the fast searcher 120a. The following table illustrates the fact that Medlock merely describes using, at any given time, the same bit from the input data 208 for the operations of the different computing circuits 204. The times listed in the table are for reference only, and are not described in Medlock, but provide a common reference to correlate the various operations performed by the computing circuits 204 (designated in the table as CC1, CC2, CC(N-1), and CCN).

Time	Bit from Input Signal 208	Memory Block with Bit from Code Sequence 210			
		CC1	CC2	CC(N-1)	CCN
t0	203a	202a	202b	202c	202d
t1	203(a+1)	202(a+1)	202(b+1)	202(c+1) =202d	202(d+1)
…	…	…	…	…	…
tj	203b =203(a+A)	202b	202(b+A)	202(c+A) =202(e-1)	202(d+A) =202e
…	…	…	…	…	…
t(k-1)	203c =203(a+A+B)	202c	202(b+A+B)	202(c+A+B)	202(d+A+B) =202f
…	…	…	…	…	…
tk	203d =203(a+A+B+N)	202d	202(b+A+B+N)	202(c+A+B+N) =202f	202(d+A+B+N) =202g

Thus, this table illustrates that at any given time there is only one bit of the input signal 208 that is operated on with different bits from the code sequence 210. Specifically, at time t0, only bit 203a of the input signal 208 is used for the operations with the corresponding bits stored in the memory blocks 202a, 202b, 202c, and 202d. Similarly, at time tk, only bit 203d of the input signal is used for the operations with the corresponding bits stored in the memory blocks 202d, 202(b+A+B+N) (wherein A, B, and N are offsets), 202(c+A+B+N) (i.e., 202f), and 202(d+A+B+N) (i.e., 202g). Even though bits stored in multiple memory blocks of the code sequence memory 216a are used in parallel, those bits of the code sequence 210 are used in operations with only a single bit of the input signal 208. The use of a single bit at a time from the input signal 208 is evidence that Medlock does not disclose combining bits of the received input signal to form a word. In other words, there is no disclosure in Medlock of combining bits of the input signal 208 to form a word.

Furthermore, even though the various computing circuits 204 may operate on different bits of the code sequence 210 in parallel, the description of parallel operations

of the bits of the code sequence 210 does not disclose combining bits of the received input signal 208. Therefore, Medlock does not disclose combining bits of the input signal 208 to form a word.

For the reasons presented above, Medlock does not disclose all of the limitations of the claim because Medlock does not disclose combining a bit or bits of at least two samples of a received signal to form a word, as recited in the claim. Accordingly, Appellants respectfully assert claim 1 is patentable over Medlock because Medlock does not disclose all of the limitations of the claim.

Furthermore, with this proper characterization of the disclosure of Medlock, it should become more apparent why Medlock further fails to disclose carrying out word-based, hard-wired operations because Medlock fails to disclose the more fundamental limitation of forming a word in the first place. Therefore, Appellants' previous remarks in the Appeal Brief continue to apply to the faulty nature of the rejections presented for the present claims, and reference may be made to those remarks and arguments as presented in Appellants' Appeal Brief filed previously.

For the reasons presented above and in Appellants' Appeal Brief filed previously, Medlock does not disclose all of the limitations of the claim because Medlock does not disclose carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value, as recited in the claim. Accordingly, Appellants respectfully assert claim 1 is patentable over Medlock because Medlock does not disclose all of the limitations of the claim.

Appellants respectfully assert independent claim 6 is patentable over Medlock at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Claim 6 recites similar subject matter as claim 1. Although the language of claim 6 differs from the language of claim 1, and the scope of claim 6 should be interpreted independently of claim 1, Appellants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 6.

Given that claims 2-5 and 7-13 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6, which are patentable over the cited reference, Appellants respectfully submit that dependent claims 2-5 and 7-13 are also patentable over the cited reference based on allowable base claims. Additionally, each of

claims 2-5 and 7-13 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 1, 2, 4, 6, 7, 9, and 11-13 under 35 U.S.C. 102(b) be withdrawn.

B. Claims 3 and 8 are patentable over Medlock and Laudel because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 3 and 8 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6, which are patentable over Medlock, Appellants respectfully submit that dependent claims 3 and 8 are also patentable over the combination of cited references based on allowable base claims. Additionally, each of claims 3 and 8 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 3 and 8 under 35 U.S.C. 103(a) be withdrawn.

C. Claims 5 and 10 are patentable over Medlock and Harrison because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 5 and 10 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6, which are patentable over Medlock, Appellants respectfully submit that dependent claims 5 and 10 are also patentable over the combination of cited references based on allowable base claims. Additionally, each of claims 5 and 10 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 5 and 10 under 35 U.S.C. 103(a) be withdrawn.

IV. CONCLUSION

For the reasons stated above, claims 1-13 are patentable over the cited references. Thus, the rejections of claims 1-13 should be withdrawn. Appellants respectfully request that the Board reverse the rejections of claims 1-13 under 35 U.S.C. 102(b) and 103(a).

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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V. CLAIMS APPENDIX

1. A method of correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code, the method comprising:

combining the bit or bits of at least two signal samples of the received signal to form a first word;

providing a second word containing bits corresponding to the replica signal; and

executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value.

2. A method according to claim 1 wherein the processing of the first and second words is done using hardwired circuitry.

3. A method according to claim 1 wherein the processing of the first and second words includes a word based XOR operation or its inverse and a summation of the results of that operation.

4. A method according to claim 1 wherein a software based instruction is executed to form the first word.

5. A method according to claim 1 wherein each sample of the spread spectrum signal contains at least one magnitude bit and a sign bit; wherein the first word is formed by combining the magnitude bit or bits of at least two signal samples; wherein a third word is formed by combining the sign bit of at least two signal samples; and wherein one or more software based instructions are executed to process the first, second and third words in order to obtain a correlation value.

6. A signal processor configured for correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code by combining the bit or bits of at least two signal samples of the received signal to form a

first word, providing a second word containing bits corresponding to the replica signal, and executing one or more software based instructions to carry out word-based, hard-wired operations to process the first and second words in order to obtain a correlation value.

7. A signal processor according to claim 6 wherein the processing of the first and second words is done using hardwired circuitry.

8. A signal processor according to claim 6 wherein the processing of the first and second words includes a word based XOR operation or its inverse and a summation of the results of that operation.

9. A signal processor according to claim 6 wherein a software based instruction is executed to form the first word.

10. A signal processor according to claim 6 wherein each sample of the spread spectrum signal contains at least one magnitude bit and a sign bit; wherein the first word is formed by combining the magnitude bit or bits of at least two signal samples; wherein a third word is formed by combining the sign bit of at least two signal samples; and wherein one or more software based instructions are executed to process the first, second and third words in order to obtain a correlation value.

11. A direct sequence spread spectrum signal receiver comprising an antenna and an RF front-end including an analogue to digital converter for receiving spread spectrum signals and outputting corresponding signal samples; and a signal processor according to claim 6.

12. A computer-readable storage medium having recorded thereon data containing instructions for performing a method according to claim 1.

13. A computer program comprising instructions stored on a memory device which, when executed by a processor, perform the method according to claim 1.